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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,173	04/22/2004	Syotaro Ono	252311US2S	6045

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,173	ONO ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *9 and 11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 10* is/are rejected.

7)☒ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 11/28/2005 has been entered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1-3, 7, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by UENO (JP2001077358A).

Ueno discloses a first 21b semiconductor region forming a drain (see claim 10) region, of a first (n) conductivity type; a second 22 semiconductor region forming a base (see claim 10) region, of a second (p) conductivity type formed on the first 21b semiconductor (DRAIN) region; a third 23 semiconductor region forming a source (see claim 10) region, of the first (n) conductivity type formed on a part of the second 22

semiconductor (BASE) region; the first 21b to third 23 semiconductor regions being formed into a MOS field-effect transistor; a fourth 20a semiconductor region of the first (n) conductivity type, arranged apart in boundary regions of the first 21b semiconductor (DRAIN) region and the second 22 semiconductor (BASE) region, and formed between the bottom surface of the trench 14 and the first 21b semiconductor (DRAIN) region, the fourth 20a semiconductor region having an impurity concentration higher (in regard to relative concentrations note paragraphs 0032,0035, 0042 and especially claim 2) than an impurity concentration of the first 21b semiconductor (DRAIN) region; a trench 14 formed to range (note figure 2) from a surface of the third 23 semiconductor (SOURCE) region to the third 23 semiconductor (SOURCE) region and the second 22 semiconductor (BASE) region, the trench 14 penetrating the third 23 semiconductor (SOURCE) region, a depth of the trench 14 being shorter than a depth of a deepest bottom portion of the second 22 semiconductor (BASE) region, and the trench 14 having no second 22 semiconductor (BASE) region under its bottom surface; a gate insulating film 25 formed on both facing side surfaces of the trench 14; first and second gate electrodes 26 formed on the gate insulating film 25 and opposed to the facing side surfaces of the trench 14, the first and second gate electrodes 26 being connected to each other at a part thereof inside the trench 14 above a non-inversion region beneath the trench 14, while separated from each other; and a first conductive material 18 (note figure 3), electrically connected to a source electrode 17, formed between the first and

second gate electrodes 26 on the side surfaces of the trench 14, with an insulating film 18 intervened between the first conductive material and the first and second gate electrodes 26. Note figures 1-3, paragraphs 0032-0042, and claims 1 and 2 of Ueno.

B. Claims 1, 4, 5, 7 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by TAKAHASHI ET AL. (5,776,812).

Takahashi et al. discloses a first 2 semiconductor region forming a drain (see claim 10) region, of a first (n) conductivity type; a second 16 semiconductor region forming a base (see claim 10) region, of a second (p) conductivity type formed on the first 2 semiconductor (DRAIN) region; a third 4 semiconductor region forming a source (see claim 10) region, of the first (n) conductivity type formed on a part of the second 16 semiconductor (BASE) region; the first 2 to third 4 semiconductor regions being formed into a MOS field-effect transistor; a fifth 17 semiconductor region of the second (p) conductivity type formed on a part of the second 16 semiconductor (BASE) region, the fifth 17 semiconductor region having an impurity concentration higher than an impurity concentration of the second 16 semiconductor (BASE) region (usual practice in the art is to refer to this high impurity region as the "back gate"); a source electrode 19 formed on the fifth 17 semiconductor region and the third 4 semiconductor (SOURCE) region; a trench 50 formed to range from a surface of the third 4 semiconductor (SOURCE) region to the third 4 semiconductor (SOURCE) region and the second 16 semiconductor (BASE) region, the trench 50 penetrating the third 4 semiconductor (SOURCE) region, a

depth of the trench 50 being shorter than a depth of a deepest bottom portion of the second 16 semiconductor (BASE) region, and the trench 50 having no second 16 semiconductor (BASE) region under its bottom surface; a gate insulating film 8 formed on both facing side surfaces of the trench 50; first and second gate electrodes 9 formed on the gate insulating film 8 and opposed to the facing side surfaces of the trench 50, the first and second gate electrodes 9 being connected to each other at a part thereof inside the trench 50 above a non-inversion region beneath the trench 50, while separated from each other; and a first conductive material (formed of a piece with source electrode 19. The difference between source electrode 19 and the first conductive film is that the first conductive film is formed inside trench 50 and over insulating film 18, while the source electrode is in contact with source 4 and back gate 17), electrically connected to the source electrode 19, formed between the first and second gate electrodes 9 on the side surfaces of the trench 50, with an insulating film 18 intervened between the first conductive material and the first and second gate electrodes 9. Note figures 1a-1b and column 10 lines 37-67 of Takahashi et al.

Allowable Subject Matter

4. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments with respect to claims 1-5,7,8, and 10 have been considered but are moot in view of the new ground(s) of rejection.

Some discussion seems apropos, regardless, regarding the scope of the claim term "separated."

"Separated" is a word that in ordinary usage takes on many meanings. It is perfectly appropriate to refer to the tines of a fork, or the fingers of one's hand, as "separated," in the sense that they are distinct. However, each tine, although "separate" from its fellows, must ultimately go where the fork goes, along with the rest of the tines. Each finger, although "separate" from its fellows, must follow its fellows.

On the other hand, "separate" sometimes takes on a meaning that implies a complete disconnection, with one following a different path altogether from another it is "separate" from. For example it is written, "When, in the course of human events, it becomes necessary for one people to dissolve the political bands which have connected them with another, and to assume among the powers of the earth the separate and equal station to which the laws of nature and of nature's God entitle them..."[1] Use of the word "separate," consistent with the meaning implied here, requires a radical disconnection.

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[1] Thomas Jefferson, Declaration of Independence

Patent claims construed during examination should be given their broadest reasonable interpretation consistent with the specification, and should be read in light of the specification as it would be interpreted by person of skill in art, since this policy serves public interest by reducing possibility that claims, finally allowed, will be given broader scope than is justified. In re American Academy of Science Tech Center, 70 USPQ2d 1827, Decided May 13, 2004.

In this case the meaning of "separated" is clear when read in light of the specification. In paragraph 50, for example, Applicant writes "in the above first to third embodiments, as shown in FIG. 10, a part 33, which is a part of two polysilicon wirings forming the two gate electrodes 18 and connects the two polysilicon wirings, is formed by leaving polysilicon between the two polysilicon wirings." In other words, in the first to third embodiments, the two "separate" gate electrodes 18, and a connecting part 33, are all formed of a single piece of polysilicon. Further, in dependent claim 7, applicant writes "the separated first and second gate electrodes being connected to each other at a part thereof inside the trench..." (Emphasis added). In claim 8, applicant goes on: "... the separated first and second gate electrodes are connected..."

Clearly, when applicant writes, "the first and second gate electrodes being separated from each other," he means that the two gate electrodes are "distinct," but not "disconnected." "Separated," in other words, as the tines of a fork, or the fingers on one's hand, are "separated."

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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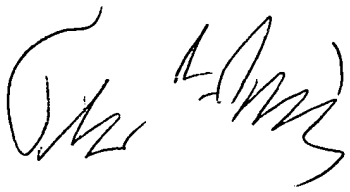
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
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01/06